// VerilogA for ADC\_FinalProject, B\_1p5stage\_VerilogA, veriloga

`include "constants.vams"

`include "disciplines.vams"

module B\_1p5stage\_VerilogA(vin,vrefp,vrefm,ph1,ph2,vcm,vout,D1,D0,vdd,vss);

parameter real clk\_th=0.9;

parameter real delay = 0;

parameter real ttime = 1p;

inout vdd,vss;

input vin,vrefp,vrefm,ph1,ph2,vcm;

output vout,D1,D0;

electrical vdd,vss;

electrical vin,vrefp,vrefm,ph1,ph2,vcm;

electrical vout,D1,D0;

real dd1,dd0,vvout;

analog begin

@(cross(V(ph1) - clk\_th, +1)) begin

if (V(vin)>V(vrefp)) begin

dd1 = V(vdd); dd0 = V(vss);

end

else if (V(vin)<V(vrefp)) && (V(vin)>V(vrefm)) begin

dd1 = V(vss); dd0 = V(vdd);

end

else begin

dd1 = V(vss); dd0 = V(vss);

end

end

@(cross(V(ph2) - clk\_th, +1)) begin

if (dd1 > 0.9) begin

vvout = ((V(vin) – 0.9) \* 2) – 1;

end

else if (dd0 > 0.9) begin

vvout = (V(vin) – 0.9) \* 2;

end

else begin

vvout = ((V(vin) – 0.9) \* 2) + 1;

end

end

V(D1) <+ transition(dd1,delay,ttime);

V(D0) <+ transition(dd0,delay,ttime);

V(vout) <+ transition(vvout,delay,ttime);

end

endmodule